IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

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Conductive Lines, Coaxial Lines, Integrated Circuitry, And Methods Of Forming Conductive Lines, Coaxial Lines, And Integrated Circuitry

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TECHNICAL FIELD

This invention relates to methods of forming conductive lines, such as co-axial lines, and to integrated circuitry incorporating conductive lines.

BACKGROUND OF THE INVENTION

As the density of integrated circuitry (IC) devices increases, continuing challenges are posed to find interconnect structures which are suitable for use with such densely-packed IC devices. For example, as clock cycles increase, interconnect structures which are capable of handling such clock cycles become necessary. Further, such interconnect structures must overcome concerns associated with signal propagation times, crosstalk, increased system noise and other spurious electrical effects which are detrimental to the performance of integrated circuits.

This invention arose out of concerns associated with providing integrated circuitry interconnect structures which are suitable for use with densely-packed, high-speed integrated circuitry devices.

SUMMARY OF THE INVENTION

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Conductive lines, such as co-axial lines, integrated circuitry incorporating such conductive lines, and methods of forming the same are described. In one aspect, a substrate having an outer surface is provided. A masking material is formed over the outer surface and subsequently patterned to form a conductive line pattern. An inner

conductive layer is formed within the conductive line pattern, followed by formation of a dielectric layer thereover and an outer conductive layer over the dielectric layer. Preferred implementations include forming the inner conductive layer through electroplating, or alternatively, electroless plating techniques. Other preferred implementations include forming the dielectric layer from suitable polymer materials having desired dielectric properties. A vapor-deposited dielectric layer of Parylene is one such preferred dielectric material.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 illustrates a cross-sectional view of a semiconductor wafer fragment at a preliminary processing step according to the present invention.

Fig. 2 illustrates the semiconductor wafer fragment of Fig. 1 at one processing step in accordance with one aspect of the invention subsequent to that of Fig. 1.

Fig. 3 illustrates the semiconductor wafer fragment of Fig. 1 at a processing step subsequent to that of Fig. 2.

Fig. 4 illustrates the semiconductor wafer fragment of Fig. 1 at a processing step subsequent to that of Fig. 3.

Fig. 5 is an isometric elevation of a portion of the semiconductor wafer fragment of Fig. 1 at the Fig. 4 processing step.

Fig. 6 illustrates the semiconductor wafer fragment of Fig. 1 at a processing step subsequent to that of Fig. 4, and in accordance with one embodiment of the present invention.

Fig. 7 illustrates the semiconductor wafer fragment of Fig. 1 at a processing step subsequent to that of Fig. 6.

Fig. 8 illustrates the semiconductor wafer fragment of Fig. 1 at a processing step subsequent to that of Fig. 7.

Fig. 9 illustrates the semiconductor wafer fragment of Fig. 1 at a processing step subsequent to that of Fig. 8.

Fig. 10 illustrates the semiconductor wafer fragment of Fig. 1 at a processing step subsequent to that of Fig. 9.

Fig. 11 illustrates the semiconductor wafer fragment of Fig. 1 at a processing step subsequent to that of Fig. 10.

Fig. 12 is a view taken along line 12-12 in Fig. 11.

Fig. 13 is a view taken along line 13-13 in Fig. 12.

<u>DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS</u>

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment in process is indicated generally at 15, and includes a semiconductive substrate 16 having an outer surface 18. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising

semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

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Referring to Fig. 2, conductive terminal members 20, 22, and 24 are formed over outer surface 18. Such constitute exemplary respective node locations with which electrical connection or communication is desired. In accordance with one aspect of the invention, other conductive terminal members are formed over the substrate and extend into and out of the plane of the page upon which Fig. 2 appears. Such other conductive terminal members can form, together with the illustrated terminal members, respective pairs of upstanding, spaced-apart terminal members. One such exemplary pair is shown in Fig. 11 at 20, 21 and discussed in more detail below.

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Referring to Fig. 3, a first masking material layer 26 is formed over substrate 16 and the illustrated conductive terminal members. Accordingly, first layer 26 is formed over and between conductive terminal members which lie into and out of the plane of the page upon which Fig. 3 appears. An exemplary masking material is photoresist, although other masking materials can, of course, be used.

Referring to Fig. 4, first layer 26 is patterned over outer surface 18 to form at least one, and preferably a plurality, of conductive line patterns 28, 30, and 32. In one aspect, conductive line patterns 28, 30, and 32 expose at least portions of respective conductive terminal members 20, 22, and 24 and their respective mated terminal members which define the respective pairs of upstanding terminal members mentioned above. Ideally, and with reference to Fig. 5, this forms a trough 23 through first layer 26 which extends between and joins respective terminal member pairs such as exemplary pairs 20, 21. Yet, trough 23 does not extend to surface 18. Such can be accomplished by limiting the time of light exposure of the preferred photoresist of layer 26 such that only an outermost portion is light transformed for subsequent stripping. Alternately, where layer 26 constitutes another material such as SiO_2, the formation of a trough between the silicon pairs in a manner which avoids surface 18 exposure could be achieved with a masked timed etch. An etch stop layer might also be used. Regardless, the trough formation enables the spaced-apart conductive terminal members, such as terminal members 20, 21, to be electrically connected through the respective conductive line patterns, as will become apparent below.

Referring to Fig. 6, and in accordance with a first preferred implementation, a first conductive layer 34 is formed over substrate 16 and within conductive line patterns 28, 30, and 32. Such layer can be formed through any suitable technique. An exemplary technique is

sputtering or otherwise blanket-depositing layer 34 over the substrate. In a preferred aspect, the sputtering is conducted in connection with an ionized magnetron sputtering reactor in order to ensure adequate step coverage within the illustrated conductive line patterns. Typical and exemplary materials for layer 34 include a bi-layer comprising titanium and copper, or chromium and copper. Such layer is preferably deposited to a thickness from between about 100 to 200 nanometers. Such layer forms a so-called seed layer for an electroplating process as described below.

Referring to Fig. 7, a second conductive layer 36 is formed over substrate 16, within conductive line patterns 28, 30, and 32, and over layer 34, preferably by electroplating techniques. Together, material of first layer 34 and second layer 36 will constitute an inner conductive layer or core of material which is formed within the line patterns. Exemplary materials for layer 36 include those materials which are suitable for use in electroplating processes, such as metal-comprising materials like copper and gold. Additionally, magnetic films comprising nickel, cobalt, and iron, and suitable alloys thereof can be used.

Referring to Fig. 8, amounts of layers 34, 36 are removed to effectively electrically isolate conductive material within the respective conductive line patterns 28, 30, and 32. In a preferred aspect, the conductive material is planarized as by suitable chemical mechanical polishing thereof relative to masking layer 26. This forms individual

inner conductive layers or cores which extend between and operably connect with individual terminal members of each respective pair.

In accordance with another preferred implementation, and one which follows from the Fig. 4 construction, the conductive material which is formed or provided within conductive line patterns 28, 30, and 32 can be formed through suitable known electroless plating techniques. Accordingly, only one layer of conductive material could be formed over the substrate and within the conductive line patterns. Processing in accordance with this implementation, after the formation of the conductive material layer, would otherwise take place substantially as described herein with respect to the first implementation.

Referring to Figs. 9 and 12, masking material 26 is removed from at least around conductive material portions which extend between respective spaced-apart conductive terminal members, such as pair 20, 21 of Fig. 12. The conductive material portions comprise conductive lines 38, 40, and 42 which include other portions which are supported above, spaced from, or otherwise suspended over substrate outer surface 18 by the respective terminal members 20, 22, and 24. Accordingly, masking material is removed from elevationally below the conductive material portions which extend between the terminal members, thereby leaving such portions supported above the underlying substrate outer surface 18. Masking material 26 can be removed through any suitable technique such as oxygen plasma etching.

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Referring to Fig. 10, a dielectric layer 44 is formed over substrate 16 and at least some of the inner conductive layers comprising respective conductive lines 38, 40, and 42. Preferably, layer 44 comprises a dielectric polymer layer which is formed over and surrounds at least the respective portions of conductive lines 38, 40, and 42 which are spaced from outer surface 18 and extend between the terminal members. An example material is Parylene. Parylene desirably has a lower dielectric constant, e.g. 2.6, as compared with dielectric constants of other materials such as SiO_2 which can have dielectric constants from between 3.9 to 4.2. Such accommodates operating parameters of high speed integrated circuitry by increasing signal propagation (decreasing propagation times) and reducing interline coupling or crosstalk. The preferred Parylene material is preferably vapor phase deposited over the substrate and the respective conductive lines. Parylene and processing techniques which utilize Parylene are described in more detail in an article entitled "Low and High Dielectric Constant Thin Films for Integrated Circuit Applications", authored by Guttman et al, and presented to the Advanced Metallization and Interconnect Systems for VLSI Applications in 1996, held in Boston, Massachusetts, October 3-5, 1996, and published in May/June 1997 by Material Research Society of Pittsburgh, Pa.

Preferably, dielectric layer 44 surrounds a substantial portion of the conductive material which constitutes conductive lines 38, 40, and 42. In accordance with one aspect of the invention, the substantial

portion of such material constitutes that portion of material which is suspended above outer surface 18. Such is more easily seen when Figs. 10 and 12 are viewed together.

Referring to Fig. 11, an outer conductive sheath 46 is formed over dielectric layer 44. Preferably, conductive sheath 46 constitutes a metal-comprising layer of material formed by chemical vapor deposition. Aluminum is an example preferred material. Layer 46 forms a coaxial outer conductive line component which is formed over dielectric layer 44.

Referring to Figs. 12 and 13, an exemplary upstanding pair of conductive terminal members 20, 21 (Fig. 12) are shown which illustrate a portion of conductive line 38 which is suspended above substrate outer surface 18. A portion of Fig. 12 has been broken away for clarity.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.